the conductivity is not less than $1\times10^{-13}/\Omega cm$. This indicates not only the improvement in breakdown voltage characteristic by the electric field shield effect but also that the device breakdown voltage characteristic is stabilized by the use of the semi-insulation surface protective film **14** with the conductivity of not less than 1×10^{-13} /Ωcm. This increases the degree of freedom to determine the guard ring structure dimension and the degree of freedom of design, for example, the stable breakdown voltage characteristic independent of variations in fabrication process of the guard ring structure. However, an excessively high conductivity eliminates the function of the insulating film. Thus, the conductivity of the surface protective film **14** is required to be on the order of 1×10^{-14} to 1×10^{-10} (1/Ωcm) and is preferably 1×10^{-13} to 1×10^{-11} (1/Ωcm) which permits easy control of the conductivity of the semi-insulation silicon nitride film by measuring the refractive index of the film.

Second Preferred Embodiment

FIG. **16** is a fragmentary plan view of the IGBT according to a second preferred embodiment of the present invention. FIG. **17** is a fragmentary cross-sectional view taken along the line XVII—XVII of FIG. **16**.

Referring to FIGS. **16** and **17**, the IGBT comprises the surface protective film **14** formed in the gate wiring area **32** and the device peripheral area **30**.

The emitter electrode **10** is electrically isolated from the gate interconnection line **9** by a narrow trench. The emitter electrode **10** and the gate interconnection line **9** which are Al—Si sputtering film are easily scratched, for example, when the semiconductor device is handled by a handling device during the fabrication process, resulting in shorting of the emitter electrode **10** and the gate interconnection line **9**. However, such a failure is prevented by the surface protective film **14** extending to the surface of the narrow trench. In addition, since there is no channel regions serving as cells under the gate wiring area **32**, the covering of the semi-insulation surface protective film **14** of silicon nitride formed by the P-CVD process and containing a large amount of hydrogen atoms does not cause the V_{th} variations. Therefore, an electrically highly stable IGBT is accomplished, with shorting of the emitter electrode **10** and the gate interconnection line **9** being prevented, like the first preferred embodiment.

Further, an electrically highly stable MOSFET is accomplished, with shorting of the emitter electrode **10** and the gate interconnection line **9** being prevented, like the first preferred embodiment by the provision of the surface protective film **14** in the gate wiring area **32** and the device peripheral area **30** of the MOSFET.

Third Preferred Embodiment

The third preferred embodiment according to the present invention includes an IGBT device structure identical with the conventional structure of FIG. **19** but fabricated by the process corresponding to that of FIG. **5** and FIGS. **6** to **12**.

Specifically, the third preferred embodiment is similar to the first preferred embodiment in the process steps between the formation of the semiconductor body **4** (FIG. **6**) and the electrode formation by Al—Si sputtering (FIG. **11**). Then radiation is performed for lifetime control, and heat treatment is performed to eliminate distortion, and the surface protective film **14** is finally formed on the device top surface.

The surface protective film **14** on the device top surface is a semi-insulation silicon nitride film formed by the P-CVD process to cover the IGBT surface except the emitter wire bonding region **13**, the gate interconnection line, and the gate bonding pad which is a part of the gate interconnection line.

As concluded from the C-V test result that (iii) the introduction of hydrogen atoms is permitted after the radiation for lifetime control and heat treatment for distortion elimination in the IGBT performing lifetime control, the use of the fabrication method of the third preferred embodiment allows defects generated due to the radiation to be reduced by the heat treatment to reduce the number of dangling bonds at the silicon-silicon oxide interface. The Si—H chemical bonds becomes difficult to generate at the silicon-silicon oxide interface.

For this reason, if the P-CVD nitride film containing a large amount of hydrogen atoms is provided in the cell area **31**, the number of Si—H chemical bonds is reduced at the silicon-silicon oxide interface in the cell area **31**, providing a stable interface state. Thus, there is provided an electrically highly stable IGBT of the conventional construction with a small amount of long-term V_{th} variations, wherein shorting of the emitter electrode **10** and gate interconnection line **9** is prevented, like the first preferred embodiment.

FIG. **18** is a graph for comparison of the percentage of variations in threshold voltage V_{th} between the present invention and the background art.

Referring to FIG. **18**, the percentage of variations in threshold voltage after a reverse bias test is a little over 15% and a little over 10% for the IGBT of the conventional construction having the protective film covering 90% and 70% of the cell area, respectively. The percentage of variations in threshold voltage after the reverse bias test is about 2% for the IGBT of the first preferred embodiment of the present invention having the protective film covering 0% of the cell area, and the percentage is about 2% for the IGBT of the second preferred embodiment of the present invention having the protective film covering 10% of the cell area. The first and second preferred embodiments provide the percentage generally equal to the percentage of variations in threshold voltage for the conventional IGBT having the PSG film containing a small amount of hydrogen atoms and formed by the LP-CVD process. For the IGBT of the third preferred embodiment having the protective film covering 75% of the cell area and fabricated by the process of performing radiation, performing heat treatment for distortion elimination, and then forming the silicon nitride surface protective film by the P-CVD process, the percentage of variations in threshold voltage is a little higher than but generally equal to the percentages of the first and second preferred embodiments.

In this manner, the first, second and third preferred embodiments achieve the electrically highly stable semiconductor device with the MOS gate having a satisfactory breakdown voltage characteristic.

The above-mentioned preferred embodiments describe the power semiconductor device having the MOS gate. However, the present invention is also applicable to semiconductor integrated circuit devices, such as memories, having an MOS gate.

While the invention has been shown and described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is therefore understood that numerous modifications and variations can be devised without departing from the scope of the invention.

What is claimed is:

1. A semiconductor device comprising:

a first semiconductor layer of a first conductivity type having first and second major surfaces;

a first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first semiconduc-

tor layer is exposed in a peripheral portion of said first major surface and said first semiconductor layer is exposed in the form of an insular region in a central portion of said first major surface;

a second semiconductor region of the first conductivity type formed in a surface of said first semiconductor region, with a channel region provided between said second semiconductor region and said insular region of said first semiconductor layer;

a gate insulating film formed on a surface of said channel region;

a first gate formed on said gate insulating film;

an interlayer insulating film formed at least on said first gate:

a first main electrode formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being electrically connected to said second semiconductor region and having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of ~~said first semiconductor layer; and~~

an integral semi-insulating plasma CVD nitride film covering at ~~least the peripheral portion of said~~ first major surface other than the central portion of said first major surface and not extending to an upper portion of said first gate, said integral semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.

2. The semiconductor device of claim 1, wherein said plasma CVD nitride film extends from the peripheral portion of said first major surface to a surface of said first main electrode at said end.

3. (Amended) The semiconductor device of claim 1, further comprising:

a second gate not covered with said first main electrode [gate]; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected [by said gate interconnection line].

4. The semiconductor device of claim 3, wherein said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

5. The semiconductor device of claim 4, wherein said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} (1/Ωcm).

6. The semiconductor device of claim 4, wherein said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} (1/Ωcm).

7. The semiconductor device of claim 1, further comprising:

a second semiconductor layer of the second conductivity type formed between said second major surface of said first semiconductor layer and said second main electrode.

8. (Amended) The semiconductor device of claim 7, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate electrode and said second gate electrode are integrally formed and electrically connected [by said gate interconnection line].

9. (Amended) The semiconductor device of claim 8, wherein

said [surface protective film] plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

10. The semiconductor device of claim 9, wherein said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} (1/Ωcm).

11. The semiconductor device of claim 9, wherein said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} (1/Ωcm).

12. A semiconductor device comprising:

a first semiconductor layer of a first conductivity type having first and second major surfaces;

at least one first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first semiconductor layer is exposed in a peripheral portion of said first major surface and said first semiconductor layer is exposed in the form of a plurality of insular regions in a central portion of said first major surface;

a plurality of second semiconductor regions of the first conductivity type formed in a surface of said at least one first semiconductor region, with channel regions provided between said second semiconductor regions and said insular regions of said first semiconductor layer;

a gate insulating film formed on a surface of said channel regions;

a first gate formed on said gate insulating film;

an interlayer insulating film formed at least on said first gate:

a first main electrode formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being electrically connected to said plurality of second semiconductor regions, said first main electrode further having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of said first semiconductor layer; and

an integral semi-insulating plasma CVD nitride film for covering at least the peripheral portion of said first major surface other than the central portion of said first major surface and not extending to an upper portion of said first gate, said integral semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.

13. The semiconductor device of claim 12, wherein said plasma CVD nitride film extends from the peripheral portion of said first major surface to a surface of said first main electrode at said end.

14. (Amended) The semiconductor device of claim 13, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected [by said gate interconnection line].

15. The semiconductor device of claim 14, wherein said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

16. The semiconductor device of claim 15, wherein said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} (1/Ωcm).

17. The semiconductor device of claim 15, wherein said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} (1/Ωcm).

18. The semiconductor device of claim 13, further comprising:

a second semiconductor layer of the second conductivity type formed between said second major surface of said first semiconductor layer and said second main electrode.

19. (Amended) The semiconductor device of claim 18, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected [by said gate interconnection line].

20. The semiconductor device of claim 19, wherein said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

21. The semiconductor device of claim 20, wherein said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} (1/Ωcm).

22. The semiconductor device of claim 20, wherein said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} (1/Ωcm).

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